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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,686	01/05/2004	Kai-Chi Chen	11844-US-PA	1685

31561 7590 04/26/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER
THAI, LUAN C

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 04/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,686	CHEN ET AL.	
	Examiner	Art Unit	
	Luan Thai	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 05 January 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3, 5, 7-10, 12, 18, and 20-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Smith (6,437,240).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1, 9, 10 and 22, Smith (see specifically figure 25) disclose a chip package structure, comprising: a packaging substrate (1512), a chipset (1524a-1524b), set over and electrically connected to the carrier (1512) via solder bump (1550a), wherein the chipset comprises a plurality of chips (1524a-1524b), at least one of the chips is bonded to the carrier in a flip-chip bonding process so that a flip-chip bonding gap is created, a heat sink (1542), set over the chipset, wherein the heat sink has a surface area greater than the chipset (see figure 25), and an encapsulating material layer (1534), filling the flip-chip bonding gap and covering the heat sink and the carrier. Although the chip package structure of Smith does not teach that *the encapsulating material layer is formed in a simultaneous molding process*, this limitation is

taken to be a product by process limitation, and it is the patentability of the claimed product and not of recited process steps, which must be established. Therefore, when the prior art discloses a product, which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324,326(CCPA 1974); In re Marosi et al., 218 USPQ 289,292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964,966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process " claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claim in "product by process" claim or not.

Regarding claims 3 and 12, the chip package structure of Smith further comprises a thermal conductive adhesive layer (1550b) set between the top surface of the chipset and the heat sink.

Regarding claims 5 and 18, wherein the encapsulating material (1534) comprises resin.

Regarding claims 7 and 20, wherein the package further comprises an array of solder balls (1518) attached to a carrier (1512) surface away from the chipset.

Regarding claims 8 and 21, wherein the package further comprises a passive component (1580) set on and electrically connected to the carrier (1512).

3. Claims 1, 3, 5-7, 9, 10, 12, 14-15, 18-20 and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Hoffman et al. (6,737,750).

Regarding claims 1, 3, 5-7, 9, 10, 12, 18-20 and 22, Hoffman et al. (see specifically figures 11 and 13) disclose a chip package structure, comprising: a packaging substrate (10), a chipset comprising a plurality of chips (12/16) set over and electrically connected to the carrier (10), wherein at least one of the chips is bonded to the carrier in a flip-chip bonding process so that a flip-chip bonding gap is created, a heat sink (14/35) of metal having a surface area greater than the chipset and bonded to the chipset via a thermal conductive adhesive layer (30/46), an encapsulating material of resin (19) filling the flip-chip bonding gap (see figure 11) and covering the heat sink and the carrier, an array of solder balls (15) attached to a carrier (10) surface away from the chipset. Hoffman et al. further teach the chipset at least comprising (see figure 13) a first chip (12), having an active surface with a plurality of first bumps thereon, wherein the first active surface of the first chip is bonded and electrically connected to the carrier (10) in a flip-chip bonding process such that the first bumps between the first chip (12) and the carrier (10) set up a flip-chip bonding gap; a second chip (16), having a second active surface, wherein the second chip (16) is attached to the first chip (12) such that the second active surface is positioned away from the first chip; a plurality of conductive wires with ends electrically connected to the second chip (16) and the carrier (10) respectively.

Although the chip package structure of Hoffman et al. does not teach that the encapsulating material layer is *formed in a simultaneous molding process*, this limitation is taken to be a product by process limitation, and it is the patentability of the claimed product and not of recited process steps, which must be established. Therefore, when the prior art discloses a

product, which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324,326(CCPA 1974); In re Marosi et al., 218 USPQ 289,292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964,966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process " claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claim in "product by process" claim or not.

Regarding claims 14-15, Hoffman et al. further teach the chipset at least comprising (see figure 11) a first chip (12), having a first active surface, wherein the first chip is attached to the carrier (10) such that the first active surface is positioned away from the carrier, and a second chip (16), having a second active surface with a plurality of bumps thereon, wherein the second active surface of the second chip (16) is bonded and electrically connected to the first chip (12) in a flip-chip bonding process such that the bumps between the second chip (16) and the first chip (12) set up a flip-chip bonding gap, and wherein the chipset further comprises a plurality of conductive wires (18) with ends connected electrically to the first chip (12) and the carrier (10) respectively.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 6 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith (6,437,240) in view of Ikeda (6,518,666).

In regard to claims 6 and 19, Smith discloses all of the claimed limitations as mentioned above except the heat sink being made of a metallic material.

A heat sink is obviously and commonly made of metal, for example, copper and aluminum are widely used at the time. For instance, Ikeda, in fig. 5, discloses an analogous package including a semiconductor chip (1) mounted on a substrate (2), and a heat sink (10) made of metal such as aluminum since aluminum is excellent in a radiation characteristic. See col. 5, lines 4+.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to recognize the material as taught by Ikeda in order to increase heat transfer ability of the heat sink since aluminum is excellent in a radiation characteristic.

6. Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith (6,437,240) in view of Nishioka et al. (JP-02000195994A).

In regard to claims 4 and 13, Smith discloses the claimed limitations as mentioned above except for specifying the thermal conductivity of the encapsulating material to be greater than 1.2W/m.K.

Nishioka et al. while related to a similar encapsulating material design teach that a sealing resin composition having a thermal conductivity not smaller than 4.0 W/m.K is used as an encapsulating material to improve heat conductivity and flame resistance (see the Abstract). It

would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the encapsulating material, as taught by Nishioka et al., to Smith's in order to improve heat conductivity and flame resistance of the semiconductor device.

7. Claims 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoffman et al. (6,737,750).

Regarding claims 16-17, Hoffman et al. disclose the claimed invention including the chipset at least comprising (see figure 13) a first chip (12), having an active surface with a plurality of first bumps thereon, wherein the first active surface of the first chip is bonded and electrically connected to the carrier (10) in a flip-chip bonding process such that the first bumps between the first chip (12) and the carrier (10) set up a flip-chip bonding gap; a second chip (16), having a second active surface, wherein the second chip (16) is attached to the first chip (12) such that the second active surface is positioned away from the first chip; a plurality of conductive wires with ends electrically connected to the second chip (16) and the carrier (10) respectively, as detailed above, except for explicitly teaching a third chip bonded and electrical connected to the second chip in a flip chip bonding process.

Hoffman et al., however, do teach that every device structures, including the structures disclosed in figures 11 and 13, can having a third chip mounted thereon using the various coupling means discussed in the invention (Col. 11, lines 40-46). It would have been obvious to one of ordinary skill in the art at the time the invention was made to add a third chip mounted and flip-chip bonded to the second chip in a similar way that the chip (16) does to the chip (12) in Hoffman et al.'s device of figure 11 since such modifying has been suggested by Hoffman et

al. (Col. 11, lines 40-46). And the purpose of do in so would increase the number chips in a chip package.

8. Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoffman et al. (6,737,750) in view of Nishioka et al. (JP-02000195994A).

In regard to claims 4 and 13, Hoffman et al. disclose the claimed limitations as mentioned above except for specifying the thermal conductivity of the encapsulating material to be greater than 1.2W/m.K.

Nishioka et al. while related to a similar encapsulating material design teach that a sealing resin composition having a thermal conductivity not smaller than 4.0 W/m.K is used as an encapsulating material to improve heat conductivity and flame resistance (see the Abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the encapsulating material, as taught by Nishioka et al., to Hoffman et al.'s in order to improve heat conductivity and flame resistance of the semiconductor device.

9. Claims 2 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoffman et al. (6,737,750) in view of Huang (6,777,819).

Regarding claims 2 and 11, Hoffman et al. disclose the claimed invention as detailed above except the standoff components set over the heat sink.

Huang while related to a similar heat sink in a semiconductor package design teaches (see specifically figures 4) the standoff components (342) set over the heat sink (345) so that during a molding process, the top ends 342a) of the standoff components (342) closely abut a top wall of the molding cavity of the mold for preventing a mold resin from flashing on the other side of the

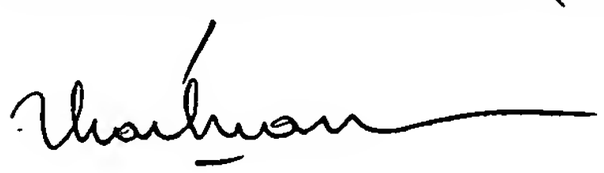
substrate (Col. 4, line 31+); and thus, the height of the standoff components (342) is equal to the thickness of the encapsulating material layer (36) over the heat sink.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the heat sink in Hoffman et al's package structure by adding a plurality of standoff components over the heat sink, as taught by Huang, in order to prevent a mold resin from flashing on the other side of the substrate, and such modification is held to be within the ordinary designing ability expected of a person skilled in the art.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is 571-272-1935. The examiner can normally be reached on 6:30 AM - 5:00 PM, Monday to Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bradley W. Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Luan Thai
Primary Examiner
Art Unit 2891
April 21, 2005